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EXAMINER

PHAM, EMILY P

ART UNIT

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2838

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

|                              |                                      |                                     |  |
|------------------------------|--------------------------------------|-------------------------------------|--|
| <b>Office Action Summary</b> | <b>Application No.</b><br>10/566,811 | <b>Applicant(s)</b><br>SPITZ ET AL. |  |
|                              | <b>Examiner</b><br>Emily Pham        | <b>Art Unit</b><br>2838             |  |

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 11 February 2010.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 9-11 and 13-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 9-11 and 13-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>01/21/2009</u> .  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. This Office Action is in response to the amendment filed on 02/11/2010.

#### ***Information Disclosure Statement***

2. The information disclosure statement (IDS) submitted on 01/21/2009 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

#### ***Claim Objections***

3. Claims 16 and 18 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 15 and 17. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

#### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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5. Claims 9-11, 13-19, 22, 23, 24, 25, 27, and 28 are rejected under 35

U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Dibugnara (USP 3,844,029).

Regarding independent claim 9: AAPA (**For example: see FIG 1, par [0003] – par [0006]**) discloses a press-fit diode **(1)**, comprising a diode chip **(7)**; a base contact **(3)** for pressing the press-fit diode **(1)** into a substrate, wherein the base contact **(3)** is attached to the diode chip **(7)** and forms a first terminal of the press-fit diode **(1)**; and a wire contact **(2, 4)** which forms a second terminal of the press-fit diode **(1)**, wherein the wire contact **(2, 4)** is attached to the diode chip **(7)**.

AAPA fails to disclose the wire contact is at least partially provided with a silver layer and the silver layer is directly applied on a nickel layer.

However, Dibugnara (**For example: see lines 30-32 of col. 10**) teaches the wire contact at least partially **(the exposed end of wire)** provided with a silver layer **(silver layer)** and the silver layer **(silver layer)** is directly applied on a nickel layer **(nickel layer)**. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the press-fit diode of AAPA to include the wire contact at least partially provided with a silver layer by Dibugnara, for the purpose of providing necessary soldering characteristics.

Additionally, since AAPA and Dibugnara are from the same field of endeavor, the purpose taught by Dibugnara would have been recognized in the pertinent arts of AAPA.

Regarding claim 10: AAPA (**For example: see FIG 1**) discloses a section of the wire contact attached to the diode chip is not provided with the silver layer.

Regarding claim 11: AAPA (**For example: see FIG 1**) discloses the base contact is not provided with a silver layer.

Regarding independent claim 13: AAPA (**For example: see FIG 1, par [0003] – par [0006]**) discloses a method for manufacturing a press-fit diode, comprising: providing a diode chip; providing a base contact configured for pressing the press-fit diode into a substrate, wherein the base contact forms a first terminal of the press-fit diode; providing a wire contact which forms a second terminal of the press-fit diode, fixedly connecting the wire contact, the base contact, and the diode chip to one another.

AAPA fails to disclose the wire contact is at least partially provided with a silver layer and the silver layer is directly applied on a nickel layer.

However, Dibugnara (**For example: see lines 30-32 of col. 10**) teaches the wire contact at least partially (**the exposed end of wire**) provided with a silver layer (**silver layer**) and the silver layer (**silver layer**) is directly applied on a nickel layer (**nickel layer**). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the press-fit diode of AAPA to include the wire contact at least partially provided with a silver layer by Dibugnara, for the purpose of providing necessary soldering characteristics.

Additionally, since AAPA and Dibugnara are from the same field of endeavor, the purpose taught by Dibugnara would have been recognized in the pertinent arts of AAPA.

Regarding claim 14: AAPA (**For example: see FIG 1**) discloses a section of the wire contact attached to the diode chip is not provided with the silver layer.

Regarding claims 15 and 16: AAPA (**For example: see FIG 1**) discloses the base contact is not provided with a silver layer.

Regarding claims 17 and 18: AAPA (**For example: see FIG 1, paragraph [0006]**) discloses the wire contact is made of copper, and the wire contact is further provided with a nickel layer

AAPA fails to disclose the silver layer is applied on a nickel layer.

However, However, Dibugnara (**For example: see lines 30-32 of col. 10**) teaches the silver layer (**silver layer**) is applied on a nickel layer (**nickel layer**). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the press-fit diode of AAPA to include the wire contact with a silver layer applied on a nickel layer by Dibugnara for the purpose of providing necessary soldering characteristics.

Additionally, since AAPA and Dibugnara are from the same field of endeavor, the purpose taught by Dibugnara would have been recognized in the pertinent arts of AAPA.

Regarding claims 19 and 24: AAPA fails to disclose the silver layer is applied before the press-fit diode is assembled.

However, Dibugnara (**For example: see FIG 7, FIG 9**) teaches the silver layer (**38a**) is applied before the press-fit diode (**diode**) is assembled (**FIG 9**). It would have been obvious to a person having ordinary skill in the art at the time the invention was

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made to modify the press-fit diode of AAPA to include the silver layer applied before the press-fit diode is assembled by Dibugnara for the purpose of properly coating the wire.

Additionally, since AAPA and Dibugnara are from the same field of endeavor, the purpose taught by Dibugnara would have been recognized in the pertinent arts of AAPA.

Regarding claims 20 and 25: AAPA (**For example: see FIG 1, paragraph [0003]**) discloses the press-fit diode as recited in claim 9, wherein a region for attaching the diode chip is recessed.

Regarding claims 22 and 27: AAPA (**For example: see FIG 1**) discloses a central section of the press-fit diode is sheathed in plastic (**9; For example: see par [0006]**) to protect the diode chip.

Regarding claims 23 and 28: AAPA (**For example: see par [0007]**) discloses the press-fit diode is electroplated in bulk in a drum process (**electroplated in bulk in a drum tin plating process**).

6. Finally, the following limitations of claims 19, 21, 22, 23, and 29 make them a product by process claim: a) “the silver layer is applied before the press-fit diode is assembled”; b) “the wire contact is inserted in a rack with a wire shaft pointing downward, and wherein the wire shaft is immersed in an electroplating vat” ; c) “a central section of the press-fit diode is sheathed in plastic to protect the diode chip”; d) “press-fit diode is electroplated in bulk in a drum process”; and “wherein the silver layer is applied before the press-fit diode is assembled, wherein a region for attaching the diode chip is recessed, wherein the wire contact is inserted in a rack with a wire shaft

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pointing downward, wherein the wire shaft is immersed in an electroplating vat, wherein a central section of the press-fit diode is sheathed in plastic to protect the diode chip, and wherein the press-fit diode is electroplated in bulk in a drum process". The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972); *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); *In re Fessmann*, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

7. Claims 21, 26, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Dibugnara (USP 3,844,029), and further in view of Wang et al (USP 7,361,257).



Regarding claims 21 and 26: AAPA fails to disclose the wire contact is inserted in a rack with a wire shaft pointing downward, and wherein the wire shaft is immersed in an electroplating vat.

However, Wang et al (**For example: see FIG 13, lines 52-53 of col. 14**) teaches the wire contact (**electrode**) is inserted in a rack (**170**) with a wire shaft (**shaft of electrode**) pointing downward, and wherein the wire shaft (**shaft of electrode**) is immersed (**For example: see line 19 of col. 17: partially immersed**) in an electroplating vat (**electrolyte bath**). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the press-fit diode of AAPA to include the wire contact inserted in a rack with a wire shaft pointing downward and the wire shaft immersed in an electroplating vat by Wang et al for the purpose of effectively coating the wire shaft.

Additionally, since AAPA and Wang et al are from the same field of endeavor, the purpose taught by Wang et al would have been recognized in the pertinent arts of AAPA.

Regarding claim 29: AAPA (**For example: see FIG 1**) discloses a region for attaching the diode chip is recessed, a central section of the press-fit diode (**1**) is sheathed in plastic (**9**) to protect the diode chip (**7**), and the press-fit diode (**1**) is electroplated in bulk in a drum process (**For example: see par [0007], electroplated in bulk in a drum tin plating process**).

AAPA fails to disclose the silver layer is applied before the press-fit diode is assembled.

However, Dibugnara (**For example: see FIG 7, FIG 9**) teaches the silver layer (**38a**) is applied before the press-fit diode (**diode**) is assembled (**FIG 9**). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the press-fit diode of AAPA to include the silver layer applied before the press-fit diode is assembled by Dibugnara for the purpose of properly coating the wire.

Additionally, since AAPA and Dibugnara are from the same field of endeavor, the purpose taught by Dibugnara would have been recognized in the pertinent arts of AAPA.

Furthermore, AAPA fails to disclose the wire contact is inserted in a rack with a wire shaft pointing downward, wherein the wire shaft is immersed in an electroplating vat.

However, Wang et al (**For example: see FIG 13, lines 52-53 of col. 14**) teaches the wire contact (**electrode**) is inserted in a rack (**170**) with a wire shaft (**shaft of electrode**) pointing downward, wherein the wire shaft is immersed in an electroplating vat (**electrolyte bath**). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the press-fit diode of AAPA to include inserting the wire contact in a rack with a wire shaft pointing downward; immersing the wire shaft in an electroplating vat by Wang et al for the purpose of effectively coating the wire shaft.

Additionally, since AAPA and Wang et al are from the same field of endeavor, the purpose taught by Wang et al would have been recognized in the pertinent arts of AAPA.

Regarding claim 30: AAPA AAPA (**For example: see FIG 1**) discloses a region for attaching the diode chip is recessed, sheathing **(9)** a central section of the press-fit diode to protect the diode chip **(7)**; wherein the press-fit diode **(1)** is electroplated in bulk in a drum process (**For example: see par [0007], electroplated in bulk in a drum tin plating process**).

AAPA fails to disclose inserting the wire contact in a rack with a wire shaft pointing downward; immersing the wire shaft in an electroplating vat.

However, Wang et al (**For example: see FIG 13, lines 52-53 of col. 14**) teaches inserting the wire contact (**electrode**) in a rack **(170)** with a wire shaft (**shaft of electrode**) pointing downward; immersing the wire shaft (**shaft of electrode**) in an electroplating vat (**electrolyte bath**). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the press-fit diode of AAPA to include inserting the wire contact in a rack with a wire shaft pointing downward; immersing the wire shaft in an electroplating vat by Wang et al for the purpose of effectively coating the wire shaft.

Additionally, since AAPA and Wang et al are from the same field of endeavor, the purpose taught by Wang et al would have been recognized in the pertinent arts of AAPA.

### ***Response to Arguments***

8. Applicant's arguments with respect to claims 9 and 13 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Loh et al (USP 6,492,725) discloses concentrically leaded power semiconductor device package and Spitz et al (USP 7,675,156) discloses electrical component with press-in diode sheathed with plastic.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

***Contact Information***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Pham whose telephone number is (571)270-3046. The examiner can normally be reached on Mon-Thu (7:00AM - 6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica Lewis can be reached on (571) 272 - 1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

May 7, 2010

/EP/  
Examiner, Art Unit 2838

/Monica Lewis/

Supervisory Patent Examiner, Art Unit 2838

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